What is claimed is:

1. A method of analyzing a waveform of a source current in a semiconductor integrated circuit including a digital circuit having a plurality of logic gates, comprising:

representing the digital circuit, according to a distribution of switching operations of the logic gates in the digital circuit, as a parasitic capacitor series which is a time series of parasitic capacitors each connected between a source line and a ground line to be charged, and a group of parasitic capacitors each charged statically;

generating an analysis model by coupling one end of the parasitic capacitor series, one end of the group of parasitic capacitors charged statically, and parasitic impedance of the source line, and connecting the other end of the parasitic capacitor series, the other end of the group of parasitic capacitors charged statically, and parasitic impedance of the ground line; and

determining the waveform of the source current in the digital circuit from the analysis model.

2. The method according to claim 1, wherein the parasitic capacitor series and the group of the parasitic capacitors statically charged are assigned for a group of the logic gates included in each segment, where the digital circuit

is divided into a plurality of segments along the border at which the parasitic impedances of the source line and the ground line are locally increased.

3. The method according to claim 1, wherein each parasitic capacitor included in the parasitic capacitor series is determined every predetermined time interval, and wherein the length of the time interval is set according to a frequency of the switching operations of the logic gates in a period of time at which the parasitic capacitors are determined.

4. The method according to claim 3, wherein the length of the time interval is set to be of shorter as the frequency of the switching operations is greater.

5. The method according to claim 1, wherein capacitance of the parasitic capacitor to be charged is calculated from input and output capacitance of the logic gates in the digital circuit to be analyzed.

6. A method of analyzing a substrate noise comprising:

regarding, as a substrate noise, a change in voltage which is caused by an interaction between the source current in the digital circuit determined from the analysis model and the parasitic impedances of the source line and the

ground line; and

using the method of claim 1 with the regarded change in voltage to analyze the substrate noise.

7. A method of designing a semiconductor integrated circuit which includes analog and digital circuits, comprising:

receiving the design specification;

designing the analog and digital circuits according to the design specification;

analyzing a substrate noise generated in the digital circuits using the method of claim 6; and

re-designing the analog and digital circuits or their layout and the location of guard bands by reviewing the result of the substrate noise analysis so that the design specification is satisfied.

8. An apparatus for analyzing a waveform of a source current in a semiconductor integrated circuit including a digital circuit having a plurality of logic gates, comprising:

arrangement for representing the digital circuit, according to a distribution of switching operations of the logic gates in the digital circuit, as a parasitic capacitor series which is a time series of parasitic capacitors each connected between a source line and a ground line to be charged, and a group of parasitic capacitors each charged statically;

arrangement for generating an analysis model by coupling one end of the parasitic capacitor series, one end of the group of parasitic capacitors charged statically, and parasitic impedance of the source line, and connecting the other end of the parasitic capacitor series, the other end of the group of parasitic capacitors charged statically, and parasitic impedance of the ground line; and

arrangement for determining the waveform of the source current in the digital circuit from the analysis model.

9. The apparatus according to claim 8, wherein the parasitic capacitor series and the group of the parasitic capacitors statically charged are assigned for a group of the logic gates included in each segment, where the digital circuit is divided into a plurality of segments along the border at which the parasitic impedances of the source line and the ground line are locally increased.

10. The apparatus according to claim 8, wherein each parasitic capacitor included in the parasitic capacitor series is determined every predetermined time interval, and wherein the length of the time interval is set according to a frequency of the switching operations of the logic gates in a period of time at which the parasitic capacitors are determined.

11. The apparatus according to claim 10, wherein the length of the time interval is set to be of shorter as the frequency of the switching operations is greater.

12. The apparatus according to claim 8, wherein capacitance of the parasitic capacitor to be charged is calculated from input and output capacitance of the logic gates in the digital circuit to be analyzed.